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L2	28320	"711"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:02
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L5	15	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:05
L6	0	(determin\$3 or check\$3 or find\$3 or identify\$3 or find\$3 or evaluat\$3) with (burst near2 lenth)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:12
L7	151	(determin\$3 or check\$3 or find\$3 or identify\$3 or find\$3 or evaluat\$3) with (burst near2 (lenth or count))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 13:12
L8	12	2 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:17

L9	4713	1 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:18
L10	23998	"713"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:21
L11	30	9 and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 12:23
L12	5063	((double adj data adj rate) or DDR) with SDRAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 12:25
L13	332	4 and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 12:30
L14	75457	"365"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 12:31
L15	29	13 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 12:49
L16	18	2 and 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 13:11

L17	219	burst near2 end near2 time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 13:11
L18	3	12 and 17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 13:11
L19	366	(determin\$3 or check\$3 or find\$3 or identify\$3 or find\$3 or evaluat\$3) with (burst near2 end)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 13:13
L20	7	12 and 19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/05 13:13
S1	2	"20050015560"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 12:49
S2	143	bae-sung\$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 12:50
S3	3	S2 and DDR	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 11:57
S4	19335	("double data rate" or DDR)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:02

S5	4450	("double data rate" or DDR) near2 SDRAM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:01
S6	2701	("double data rate" or DDR) near2 memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:02
S7	6355	("double data rate" or DDR) near2 (memory or sdram or ram or dram or ldram)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:06
S8	389	((input adj strobe) or DQS) near5 (latch or flip\$1flop or register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:07
S9	37940	((input near2 data) or DQ) near5 (latch or flip\$1flop or register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:06
S10	1017	((input near2 strobe) or DQS) near5 (latch or flip\$1flop or register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:07
S11	559	S9 and S10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:07
S12	16538	mask\$3 with (ring\$4 or glitch\$3 or noise)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:02

S13	9	S11 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 14:50
S14	6	S7 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:51
S15	309	moon-w\$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:53
S16	0	S12 and S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:52
S17	0	S7 and S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:52
S18	1258	moon-h\$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:53
S19	2	S12 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:54
S20	1	S7 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 13:54

S21	47	S7 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 14:51
S22	148746	(mask\$3 or filter\$3) with (ring\$4 or glitch\$3 or noise)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:04
S23	157	S7 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:04
S24	6	S22 and S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:05
S25	284	S7 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:06
S26	6	S10 and S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:06
S27	329	((("double data rate" or DDR) near2 (memory or sdram or ram or dram or ldram)).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:09
S28	21	S10 and S27	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/13 15:10

S29	2	"20050015560"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 07:53
S30	1	"2003-48228"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 07:55
S31	0	"KR 2003-48228"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 07:55
S32	0	"KR2003-48228"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/05 07:55


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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **400-MHz random column operating SDRAM techniques with self-skew co**
Hamamoto, T.; Tsukude, M.; Arimoto, K.; Konishi, Y.; Miyamoto, T.; Ozaki, H.;
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- ☐ 2. **A 0.18- μ m 256-Mb DDR-SDRAM with low-cost post-mold tuning method f**
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- ☐ 3. **Digital delay locked loop with open-loop digital duty cycle corrector for 1**
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Chunseok Jeong; Changsik Yoo; Jae-Jin Lee; Joongsik Kih;
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- ☐ 4. **A 390 mm² 16-bank 1 Gb DDR SDRAM with hybrid bitline architecture**
Kirihaata, T.; Mueller, G.; Ji, B.; Frankowsky, G.; Ross, J.; Terletzki, H.; Netis, D
Hanson, D.; Daniel, G.; Hsu, L.; Storaska, D.; Reith, A.; Hug, M.; Guay, K.; Sel
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- ☐ 6. **A 1.6-Gb/s/pin double data rate SDRAM with wave-pipelined CAS latency**
Sang-Bo Lee; Seong-Jin Jang; Jin-Seok Kwak; Sang-Jun Hwang; Young-Hyur Chil-Gee Lee;
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- ☐ 7. **A 2.5 V 333 Mb/s/pin 1 Gb double data rate SDRAM**
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- ☐ 8. **A 250 Mb/s 1 Gb double data rate SDRAM with a bi-directional delay and a shared redundancy scheme**
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- ☐ 9. **A 390-mm², 16-bank, 1-Gb DDR SDRAM with hybrid bitline architecture**
Kiriata, T.; Mueller, G.; Ji, B.; Frankowsky, G.; Ross, J.M.; Terletzki, H.; Netis. Weinfurtnr, O.; Hanson, D.R.; Daniel, G.; Hsu, L.L.-C.; Sotraska, D.W.; Reith, Guay, K.P.; Selz, M.; Poechmueller, P.; Hoenigschmid, H.; Wordeman, M.R.;
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- ☐ 10. **A 2.5-V, 333-Mb/s/pin, 1-Gbit, double-data-rate synchronous DRAM**
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- ☐ **13. A Source-Synchronous Double-Data-Rate Parallel Optical Transceiver IC**
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- ☐ **14. A 500 Mb/s/pin quadruple data rate SDRAM interface using a skew cancel**
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- ☐ **15. A 64-Mbit, 640-MByte/s bidirectional data strobed, double-data-rate SDRAM for a 256-MByte memory system**
Kim, C.H.; Lee, J.H.; Lee, J.B.; Kim, B.S.; Park, C.S.; Lee, S.B.; Lee, S.Y.; Park J.G.; Nam, H.S.; Kim, D.Y.; Lee, D.Y.; Jung, T.S.; Yoon, H.; Cho, S.I.;
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- ☐ **16. A register-controlled symmetrical DLL for double-data-rate DRAM**
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- ☐ **17. A 250-Mb/s/pin, 1-Gb double-data-rate SDRAM with a bidirectional delay shared redundancy scheme**
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☐ **22. A 1.2 Gb/s/pin double data rate SDRAM with on-die-termination**

Ho Young Song; Seong Jin Jang; Jin Seok Kwak; Cheol Su Kim; Chang Man Jeong; Yun Sik Park; Min Sang Park; Kyoung Su Byun; Woo Jin Lee; Young C Hwa Shin; Young Uk Jang; Seok Won Hwang; Young Hyun Jun; Soo In Cho;

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- ☐ **23. A low cost high performance register-controlled digital DLL for 1 Gbps/sd SDRAM**
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- ☐ **24. Frequency domain topology optimization methodology for a double data rate SDRAM synchronous DRAM data Interface**
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- ☐ **25. 2 metal layer tape package for improving the performance of high speed digital signal processing**
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